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QUANTA  
COMPUTER

Title

Page List

Size

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Rev

Custom

GD3 Main Board

1A

Date:

Monday, May 11, 2009

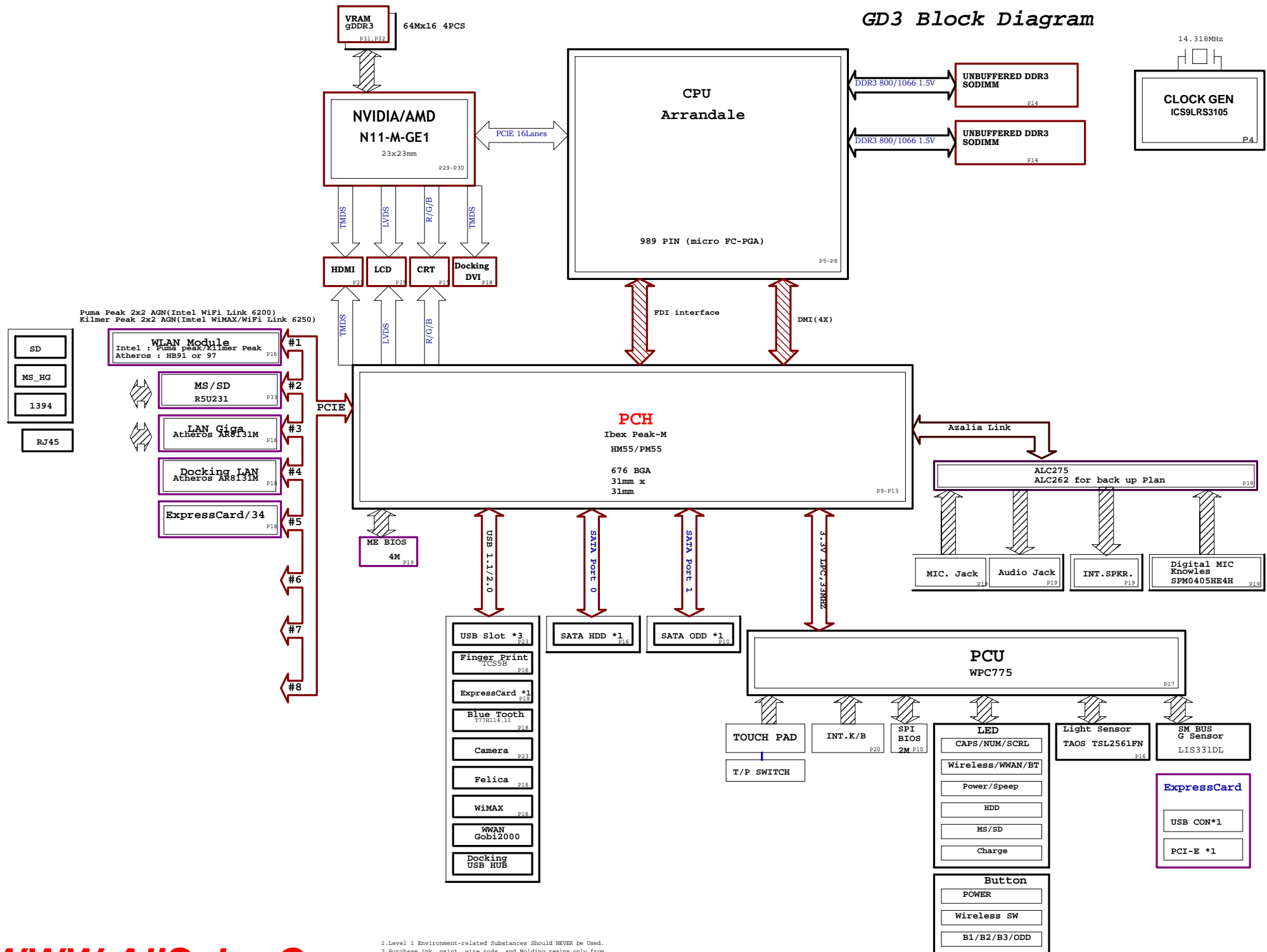
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### GD3 Block Diagram

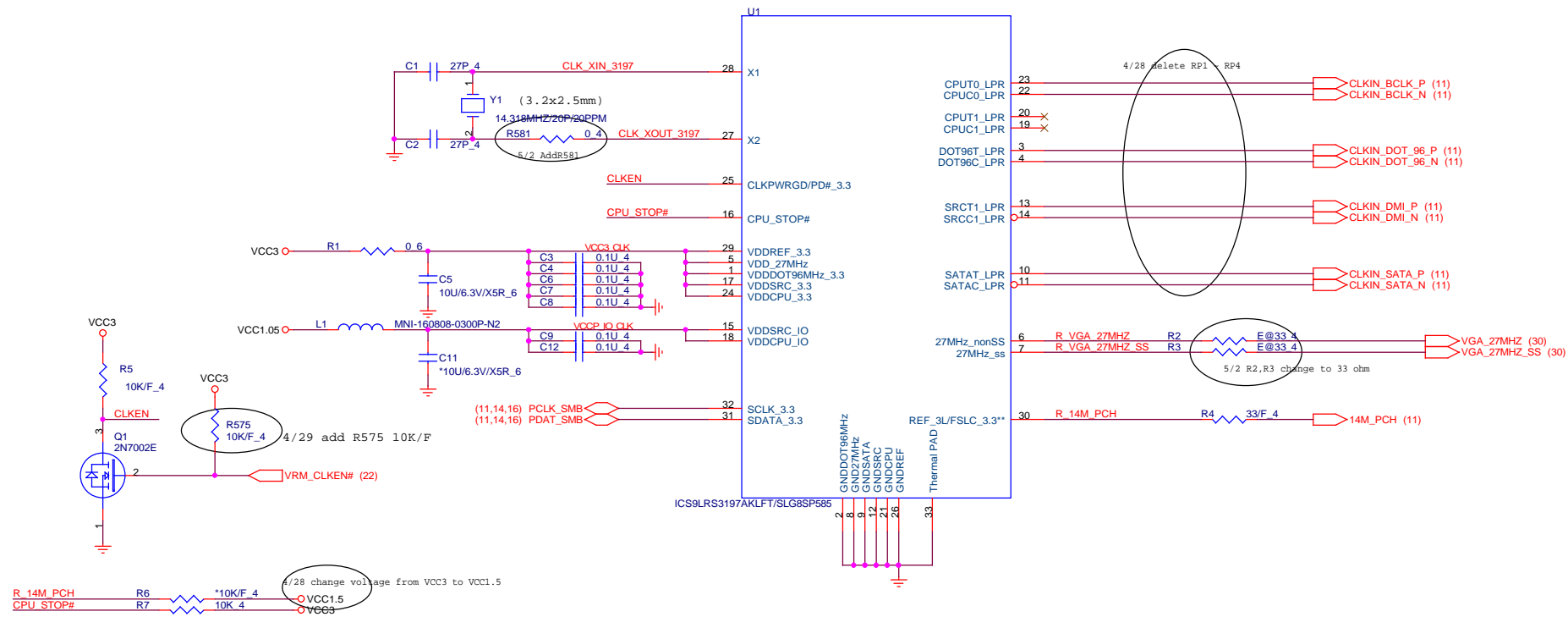


0601:  
P7 R605,R606 change PU from GND to VCC1.05

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0505:
-P18 Add AD_OVP
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0501:
- P19 Delete Q27,R346,Q25,R344,Q26,Q24; Add U59
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<p>Page 16</p> <p>CON38.60 Add USBOC1# (USB OC protection)</p> <p>Page 11</p> <p>U4,J16 add USBOC1#</p> <p>USBP2 +/- change to Docking USB (NEO request)</p> <p>USBP3+/- change to Express Card(NEO request)</p> <p>USBP4+/- change to USB PORT2(NEO request)</p> <p>USBP8+/- change to Finger Pront(NEO request)</p> <p>USBP9+/- change to Camera(NEO request)</p> <p>USBP10+/- change to WWAN(NEO request)</p> <p>USBP11+/- change to Felica(NEO request)</p> <p>USBP12+/- change to WiMAX(NEO request)</p> <p>USBP13+/- change to BT(NEO request)</p> <p>PCIE1 change to WLAN(NEO request)</p> <p>PCIE2 change to Card BUS(NEO request)</p> <p>PCIE3 change to LAN(NEO request)</p> <p>PCIE4 change to Docking LAN(NEO request)</p> <p>0330</p> <p>- P29 ~ P32</p> <p>Change</p> <p>0330phice</p> <p>19P17 Add R551 for PCIE_REQ_CARDBUS#</p> <p>19P21 Add FP_PRS#</p> <p>P19 CON44 change to 60P</p> <p>0400</p> <p>0400 Present,Add KBBL_PRESENT#</p> <p>0400</p> <p>0400 Object and Light sensor.</p> <p>0407:</p> <p>- P20 Add C691 10UF(for Light sensor)</p> <p>0408:</p> <p>P17,P20 Add KBBL_PRESENT#</p> <p>0410:</p> <p>- P9,P21 Delete DVI interface</p> <p>- P12 Add HDD_unload</p> <p>- P14 Delete Thermal IC for DDR</p> <p>- P18 Delete DVI HP resistor</p> <p>0412</p> <p>0412 Reserve CRT PRESENT)</p> <p>0415:</p> <p>-</p> <p>P9,P17</p> <p>Add</p> <p>0415 Swap DMI/FDI BUS for routing .</p> <p>SUSCUT</p> <p>0415 Delete Port 4</p> <p>0415</p> <p>0415 Delete 1.8"HDD</p> <p>0415</p> <p>0415 CONNECTOR(CON47)</p> <p>0415</p> <p>0415 U23 change BIOS size to 2MB</p> <p>- P10 U54 change BIOS size to 4MB</p> <p>- P27 PCN4 change pin defined</p> <p>- P18 change Docking connector to</p> <p>0415:</p> <p>- P7</p> <p>delete</p> <p>0415</p> <p>- P9 R120 no mount (check List)</p> <p>- P9 R80,R81 change value to 100K (check List)</p> <p>- P9 Add R567 (check list)</p> <p>- P10 R147,R149 delete(check List)</p> <p>- P10 change U54 power from 3VPCU to 3VSUS.</p> <p>- P10 Add R561,R562 for U54 pull high.(Check list)</p> <p>- P10 R508 delete(check list)</p> <p>- P10 R148,R150 change to VCC3(check List)</p> <p>- P11 change PCIE_REQ power rail to RVCC3 &amp; VCC3</p> <p>- P11 Add R560 for REQ.(check list)</p> <p>- P11 R168,R551 power to VCC3.</p> <p>- P11 R174 change to 22 ohm.(Check List)</p> <p>- P11 R161,R162,R163,R164 mount</p> <p>- P11 R169,R172 change to 47 ohm</p> <p>- P11 Add R570 for PCIEREQ(check list)</p> <p>- P12 Move SCI# from GPIO8 to GPIO6,(GPIO8 is strapping)</p> <p>- P12 R199 change power from RVCC3 to VCC3.</p> <p>- P12 R210 delete.</p> <p>- P12 KBMSI# move from GPIO15 to GPIO13</p> <p>- P12 Add R564 for GPIO28(check list)</p> <p>- P12 Add R566 for GPIO57(check list)</p> <p>- P12 Add R568,R569(check list)</p> <p>- P16 Modify CON38 Pin defined</p> <p>- P17 R315,R318 no mount</p> <p>- P17 Add R563 to GND</p> <p>- P20 Delete power reset circuit</p> <p>0422:</p> <p>- P11 Add CRT_SENSE</p> <p>- P12 add SENS_R_EN#</p> <p>- P14 Add U7 for Thermal sensor</p> <p>- P17 Delete CRT_SENSE,SENSE_EN# for CRT Plug function dropped.</p> <p>- P17 Add R571,R572 for SMBUS pull high.</p> <p>- P17 Add BAT_SDA/BAT_SCK for Battery using.</p> <p>- P17 change SDA2 net name for 35001</p> <p>- P17 change NUMLED to GPIO81</p> <p>- P17 change SCROLED to GPIO34</p> <p>- P19 CON44 add SMBUS for AMP TPA2016D2.</p> <p>- P19 CON44 add CR_LEDN_MS_SD for MS/SD LED.</p> <p>- P33 delete MSLED and move to Audio/B</p>	<p>0423:</p> <p>- P15 change camera power to 3VSUS</p> <p>- P18 CON42 pin14,15,16 change power rail</p> <p>- P19 change ODD power from VCC5 to 5VPCU</p> <p>- P19 change HDD_UNLOAD to pin18</p> <p>0424:</p> <p>- P33 add C710 for EMI</p> <p>- P15 add C711,C712 for EMI</p> <p>- P15 CON44 modify pin definieion.</p> <p>0427:</p> <p>- P15 CON4 pin3/4/5 change to GND</p> <p>- P16 Delete R559.(Q49 include R)</p> <p>0427:</p> <p>- P15 CON4 pin3/4/5 change to GND</p> <p>- P16 Delete R559.(Q49 include R)</p> <p>- P16 Add Q510 for WWAN LED</p> <p>- P17 Add BUTTON_S3</p> <p>- P18 Docking pin46 change to GND</p> <p>- P19 Delete WWAN_EN# net</p> <p>0428:</p> <p>- P4 Delete RP1 ~ RP4</p> <p>- P4 R6 change voltage from VCC3 to VCC1.5</p> <p>- P5 R22 change value from 4.7K to 1.1K</p> <p>- P5 R23 change value from 12K to 3K</p> <p>- P7 C688 change direction</p> <p>- P7 Delete R57,R58</p> <p>- P7 R47,R48 change to GND</p> <p>- P7 Add R574 for reserve</p> <p>- P7 delete VTT_SEL net</p> <p>- P8 RSVD17,18 connect to GND</p> <p>- P18 C376,C377 delete.</p> <p>- P20 Add U57,R573,C715 for KBBL current protect</p> <p>- P20 D51 mount</p> <p>- P21 Add D52,D53 for SSD protect</p> <p>- P21 Add U58 for current protect</p> <p>- P25 delete VTT_SEL circuit</p> <p>- P29 R4003 no mount.</p> <p>- P30 Add R4105</p> <p>- P33 change net name to "XOUT_231","XIN_231".</p> <p>- P33 R277 ~ R281 change from 68 to 33 ohm.</p> <p>0429:</p> <p>- P4 Add R575 10K</p> <p>- P4 Q1 change to 2N7002E</p> <p>- P5 delete R41,R40,Q6</p> <p>- P9 Delete U5,R113,R108,C144,C143</p> <p>- P9 Pin P7 add ACPRESENT</p> <p>- P11 R169,R172 change to 22 ohm</p> <p>- P11 R181 pull high to VCC1.8</p> <p>- P12 Add R577 for default</p> <p>- P10 R134 ~ R141 no mount</p> <p>- P10 Delete R143</p> <p>- P17 Add R576 for FM_SLP_S5#</p> <p>- P17 R318,R315 mount 33K ohm</p> <p>- P17 EC pin 123 add RSMRST#</p> <p>- P17 Add ACPRESENT</p> <p>- P26 Delete H_PROCHOT# for VR</p> <p>- P30 R4033~ R4039 change value from 10K to 2.2K</p> <p>0430:</p> <p>- P10 HDA_DOCK_RST# PU value change from 10K to 2.2K(Internal PD 20K)</p> <p>- P12 Delete R194</p> <p>- P12 Delete R564,Add T89 in GPIO28</p> <p>- P12 R197 change from 54.9 to 56 ohm(DG)</p> <p>- P13 Delete R213,L2,C171 for VCCACLK</p> <p>- P13 Delete L8,C211 for VCCSATAPLL</p> <p>- P13 Delete L9 for VCCFPIDPLL</p> <p>- P13 Delete L9 for VCCAPLLEXP</p> <p>- P13 DCPUSUSRP delete RVCC3 power plane</p> <p>- P13 Add R578,R579,Q51,Q52</p> <p>- P13 Add C716,C717</p> <p>- P13 Delete C176,Add R580 for VCCLAN</p> <p>- P15 CON4.30 change to VCC3</p> <p>- P18 R343 no mount</p> <p>- P18 Q23 pin2 change to DOCK_INSERT</p> <p>0501:</p> <p>- P19 Delete Q27,R346,Q25,R344,Q26,Q24; Add U59</p> <p>0502:</p> <p>- P3 Add R581 for crystal.</p> <p>- P3 R2,R3 change to 33 ohm</p> <p>- P7 Add R582 for FM_DPRSLEPVR PD.</p> <p>- P9 R80,R81 change to Ie</p> <p>- P10 Add R583</p> <p>- P10 R142 change value from 2.2K to 1K</p> <p>- P11 GPIO5 change to KBBL_PRESENT#</p> <p>- P11 U4 PIN T45,P43,T42 change to T90,T91,T92</p> <p>- P17 R345 mount 10UF</p> <p>- P17 Delete R571,R572</p> <p>- P17 U8 pin 66,119,120 change to PRS#0 ~ PRS#2</p> <p>- P27 PCN4 PIN34,36 change to MBDATA/MBCLK</p> <p>0504:</p> <p>- P9 GPIO30 change net name to "SUS_PWR_DN_ACK"</p> <p>- P12 Add R585</p> <p>- P17 Pin24 change net name to "SUS_PWR_DN_ACK"</p> <p>- P33 CON9,CON16 change footprint</p> <p>- P33 MS/SD power change to lch circuit</p>	<p>0505:</p> <p>- P18 Add AD_OVP</p> <p>0506:</p> <p>- P15 Swap Pin for Rp19</p> <p>- P16 CON38 pin 100 change from MAINON to GND</p> <p>- P17 R300,R301 change power from VCC5 to VCC3</p> <p>- P19 CON44 PIN37 change to GND</p> <p>- P19 Add CON47,L26 ~ L29,C718 ~ C721</p> <p>- P33 Add Q53,R586,D54 for MS/SD LED</p> <p>0507:</p> <p>- P16 Add U61,R589,R590,Q54 for WWAN Current Limit.</p> <p>- P16 CON46 PIN 3-5 change power from RVCC3 to 3VWAN</p> <p>- P18 Add U60,R587,C722 for TP FPC protect</p> <p>- P19 Add CON47,L26 ~ L29,C718 ~ C721</p> <p>- P19 CON44 change to 50 pin.</p> <p>- P19 CON44 Pin 37 ~ 40 add speaker net</p> <p>- P19 Add CON47 for speaker.</p> <p>- P19 U59 change to TI TPS2557</p> <p>- P19 Add R591,Q55</p> <p>0508:</p> <p>- P12 U4.Y3/C38 delete Net</p> <p>- P12 R206,R209 mount 10K</p> <p>- P12 U4.M11 change net from "HDD_UNLOAD" to VCC3.</p> <p>- P16 CON38 Pin 52 change to GND</p> <p>- P16 CON38 pin 97,99 change to 5VSUS</p> <p>- P16 CON46 pin 6,7,8 change to 3VSUS_AUX</p> <p>- P16 Add U62,R592,R593,Q56 for WLAN power</p> <p>- P17 Add R597,R598 3.3K</p> <p>- P17 Add U63,R594,R595,R596 for GPIO</p> <p>- P17 U18.114 change net to "ODD_PWEN"</p> <p>- P17 U18.6 change net to "HDD_INTERRUPT."</p> <p>- P17 U18.14 change net to "HDD_INTERRUPT1."</p> <p>- P27 PCN4 pin34,36 change net to MBCLK_BAT/MBDATA_BAT</p> <p>0509:</p> <p>- P10 R583 change portion</p> <p>- P13 Add Q58,R603</p> <p>- P15 R554 change to GND</p> <p>- P17 Add R604 for ODD_EJECT default</p> <p>- P18 Add R599 for HDMI_DOCK_HPD_EXT</p> <p>- P18 Add F8 for TP VCC3 current protect</p> <p>- P26 delete H_PROCHOT#</p> <p>- P29 Delete PR308</p> <p>- P33 Add R602</p> <p>0511:</p> <p>- P7 Add R605,R606,R607</p> <p>- P11 RP5 pin 5,10 change power from 3VSUS to RVCC3</p> <p>-</p>
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CPU Frequency Select Table

FSLC	CPU MHz	SRC MHz	REF MHz	USB MHz	DOT MHz
0 (default)	133.33	100.00	14.318	48.00	96.00
1	100.00				

Table 2: pin 6, 7 Configuration

B1b4	B1b3	B1b2	B1b1	Pin 6 MHz	Pin 7 MHz	Spread %	Comment
0	0	0	0	N/A	N/A	N/A	N/A
0	0	0	1	N/A	N/A	N/A	N/A
0	0	1	0	27MHz_nonSS	27MHz_SS	-0.5%	
0	0	1	1	27MHz_nonSS	27MHz_SS	-1%	
0	1	0	0	27MHz_nonSS	27MHz_SS	-1.5%	
0	1	0	1	27MHz_nonSS	27MHz_SS	-2%	
0	1	1	0	27MHz_nonSS	27MHz_SS	-0.75%	
0	1	1	1	27MHz_nonSS	27MHz_SS	-1.25%	
1	0	0	0	27MHz_nonSS	27MHz_SS	-1.75%	
1	0	0	1	27MHz_nonSS	27MHz_SS	+0.5%	
1	0	1	0	27MHz_nonSS	27MHz_SS	+0.75%	
1	0	1	1	N/A	N/A	N/A	N/A
1	1	0	0	N/A	N/A	N/A	N/A
1	1	0	1	N/A	N/A	N/A	N/A
1	1	1	0	N/A	N/A	N/A	N/A
1	1	1	1	N/A	N/A	N/A	N/A

Table 4: Device ID table

B8b7	B8b6	B8b5	B8b4	Comment
0	0	0	0	56 pin TSSOP
0	0	0	1	64 pin TSSOP
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	72 pin QFN
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	32 pin QFN
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

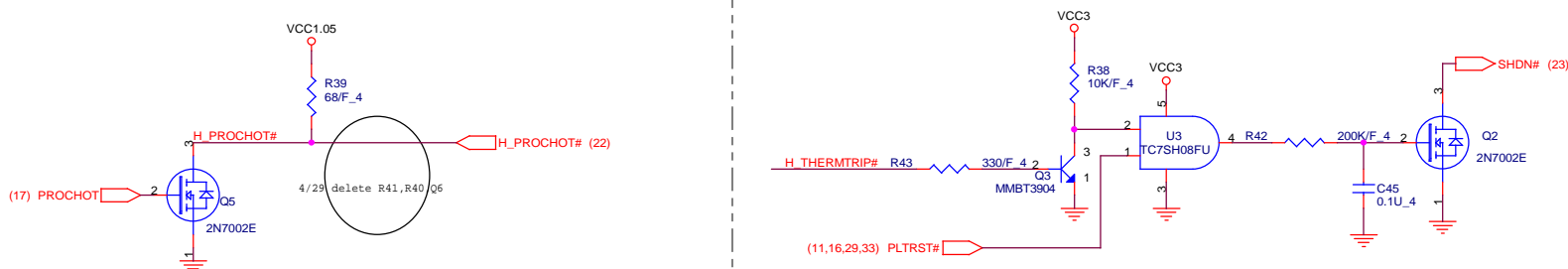
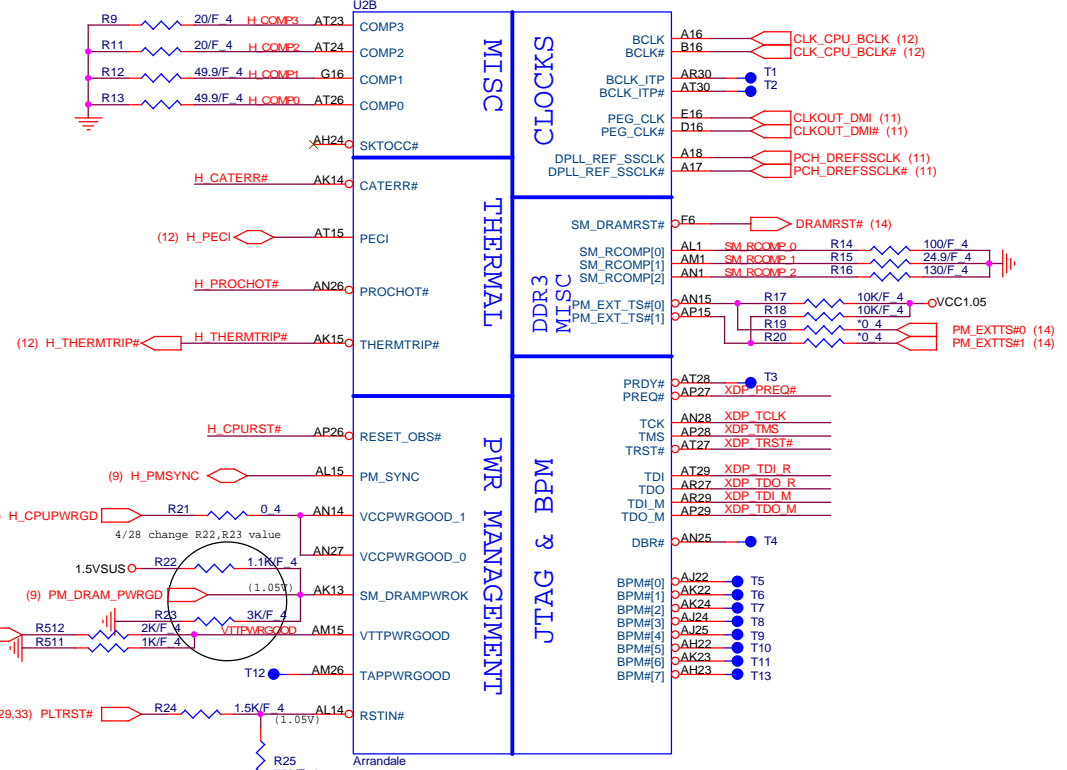
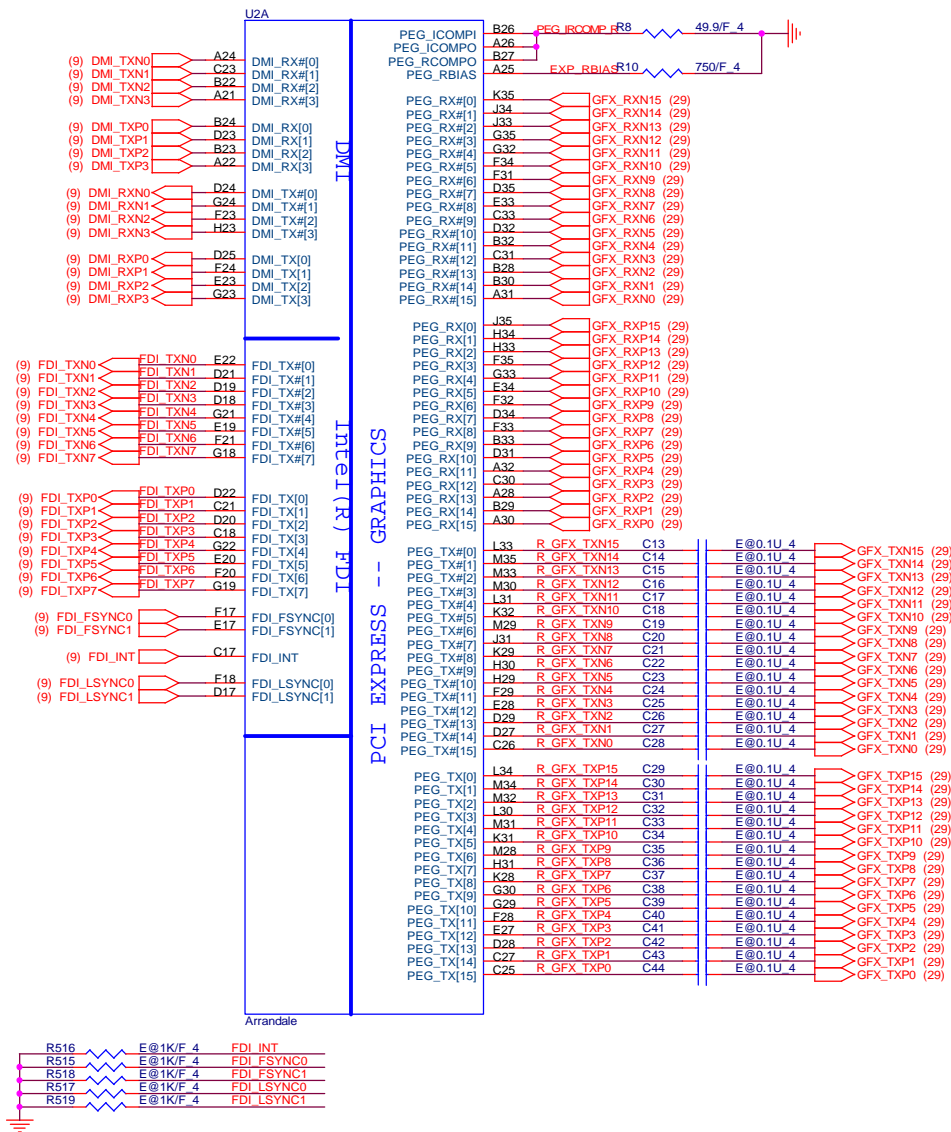
Table 3: IO Vout select table

B9b2	B9b1	B9b0	IO_Vout
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

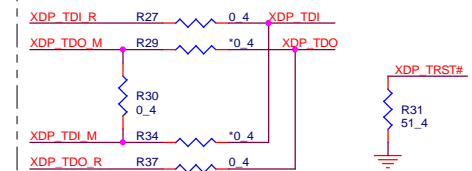
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Size:	Document Number:	Rev 1A	
GD3 Main Board			
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1.Level 1 Environment-related Substances Should NEVER be Used.

2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



## JTAG MAPPING



Scan Chain (Default)	STUFF -> R88, R89, R91 NO STUFF -> R90, R92
CPU Only	STUFF -> R88, R90 NO STUFF -> R89, R92, R91
GMCH Only	STUFF -> R92, R91 NO STUFF -> R88, R90, R89

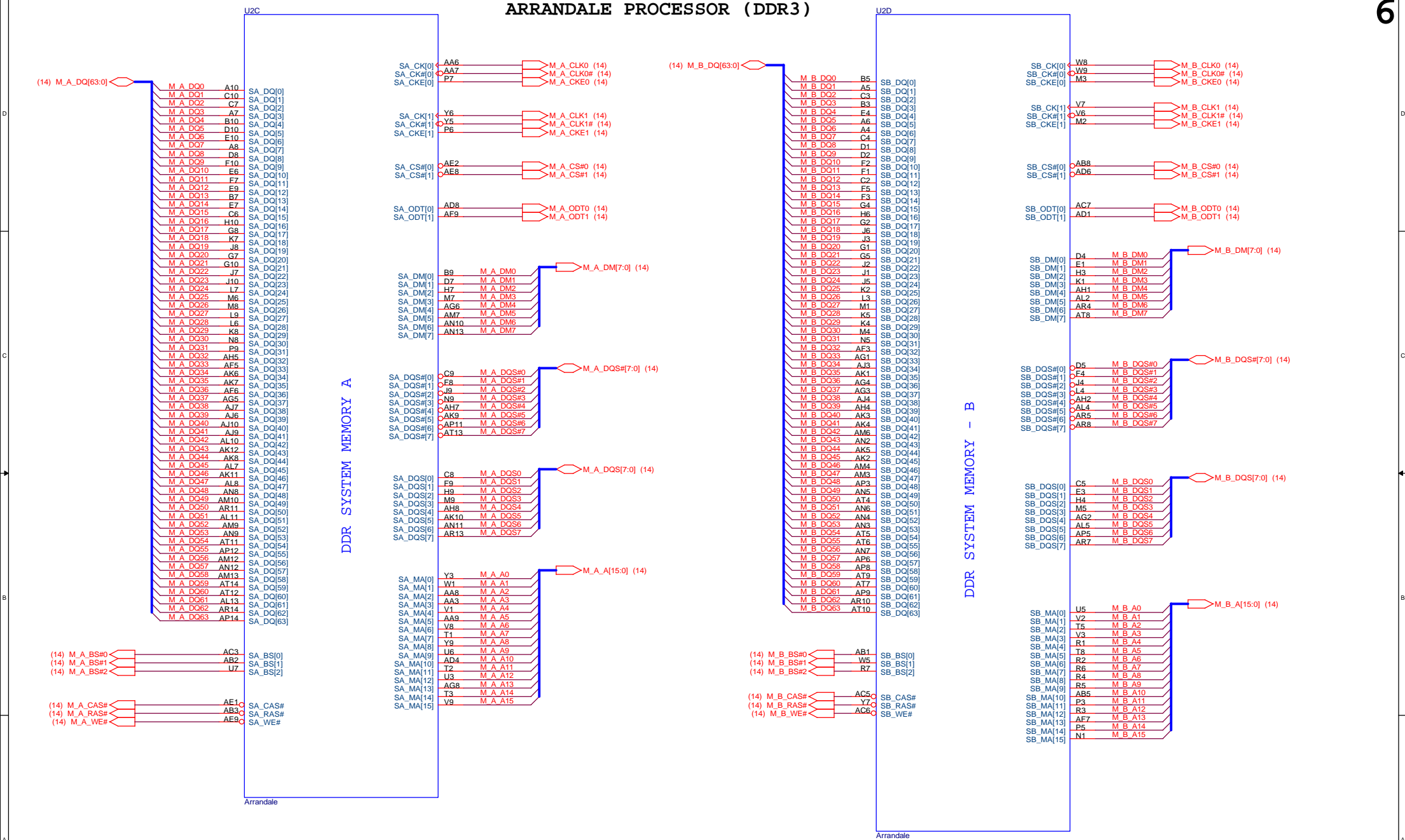


PROCESSOR 1/4(HOST&PCI)		
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- Level 1 Environment-related Substances Should NEVER be Used.
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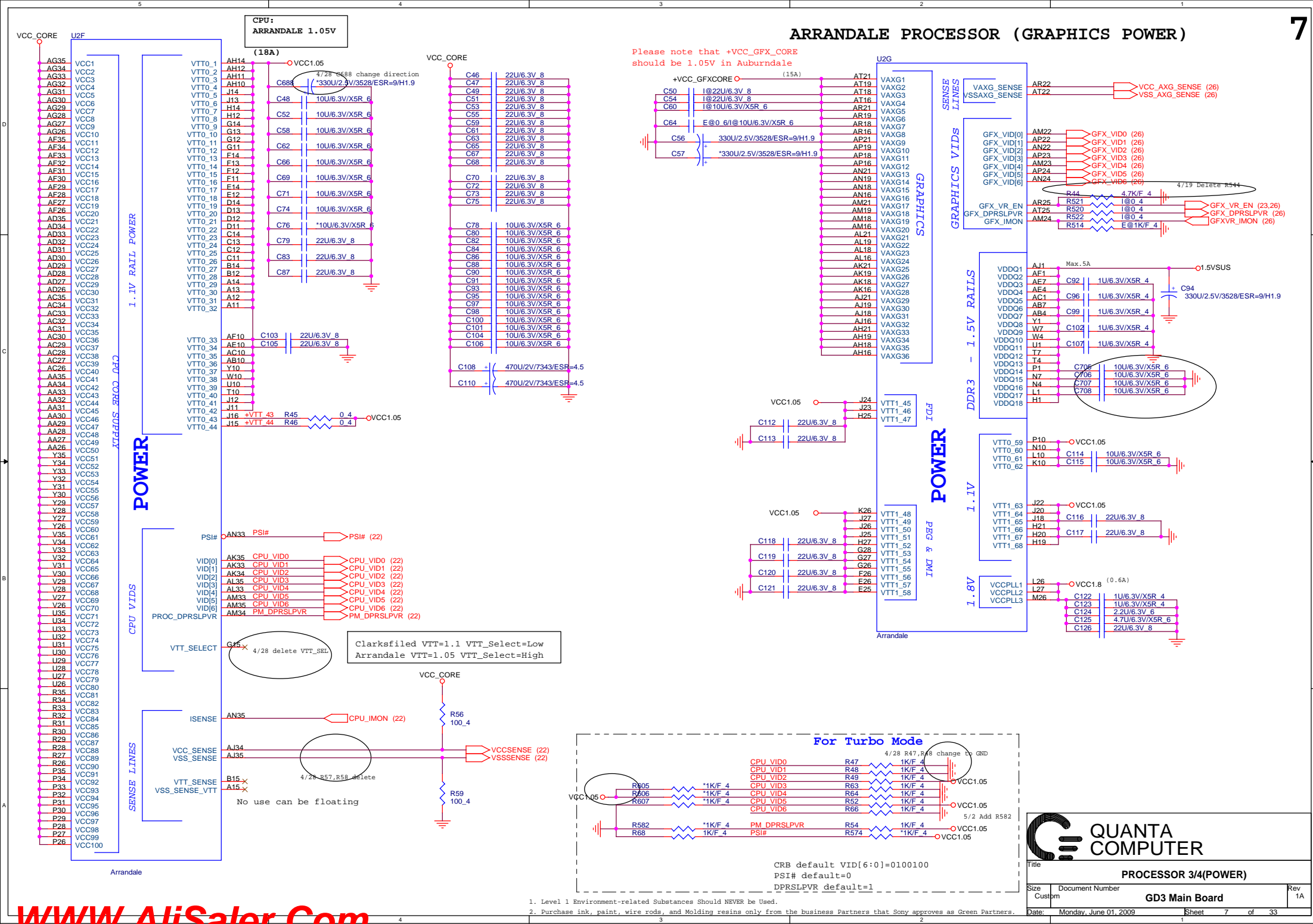
## ARRANDALE PROCESSOR (DDR3)



<b>QUANTA COMPUTER</b>		
Title		
PROCESSOR 2/4(DDR)		
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## ARRANDALE PROCESSOR (GRAPHICS POWER)

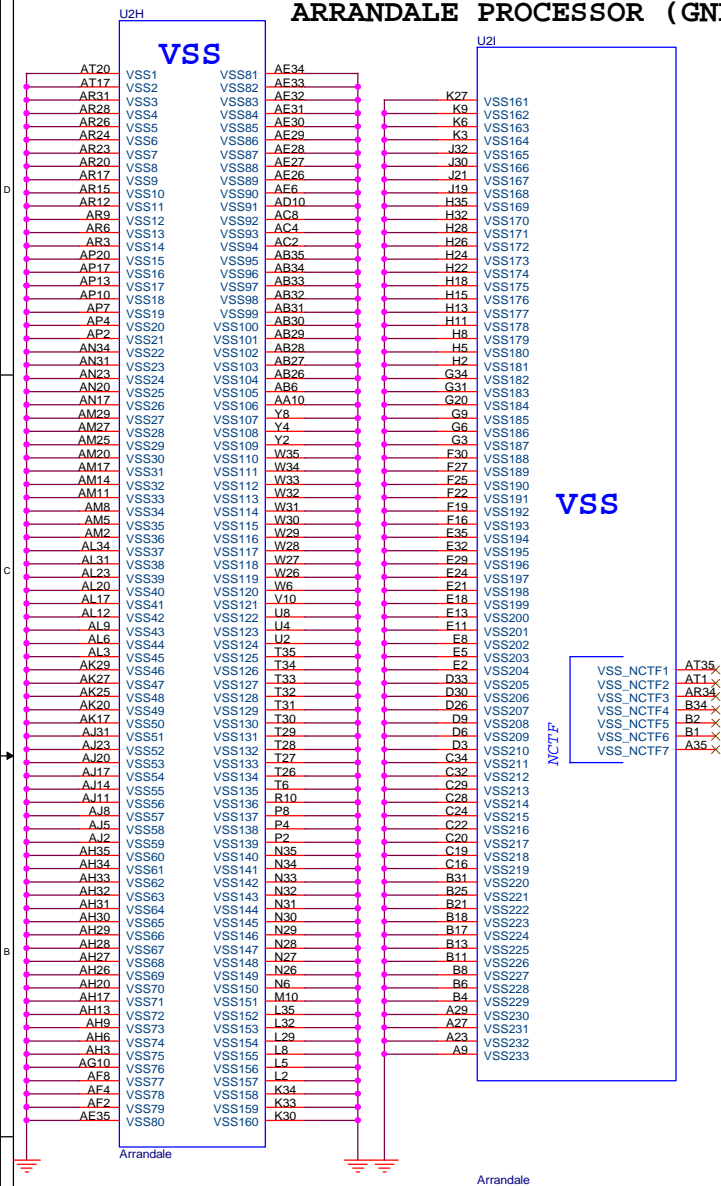




## ARRANDALE PROCESSOR (GND)

## ARRANDALE PROCESSOR( RESERVED, CFG)

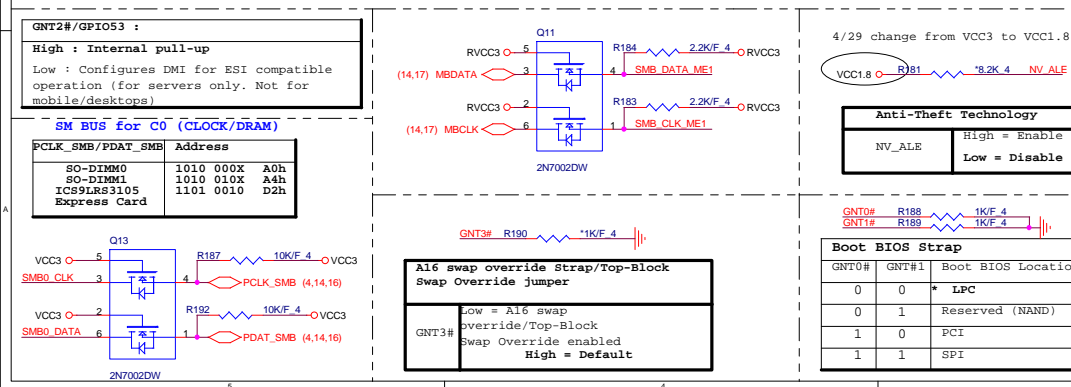
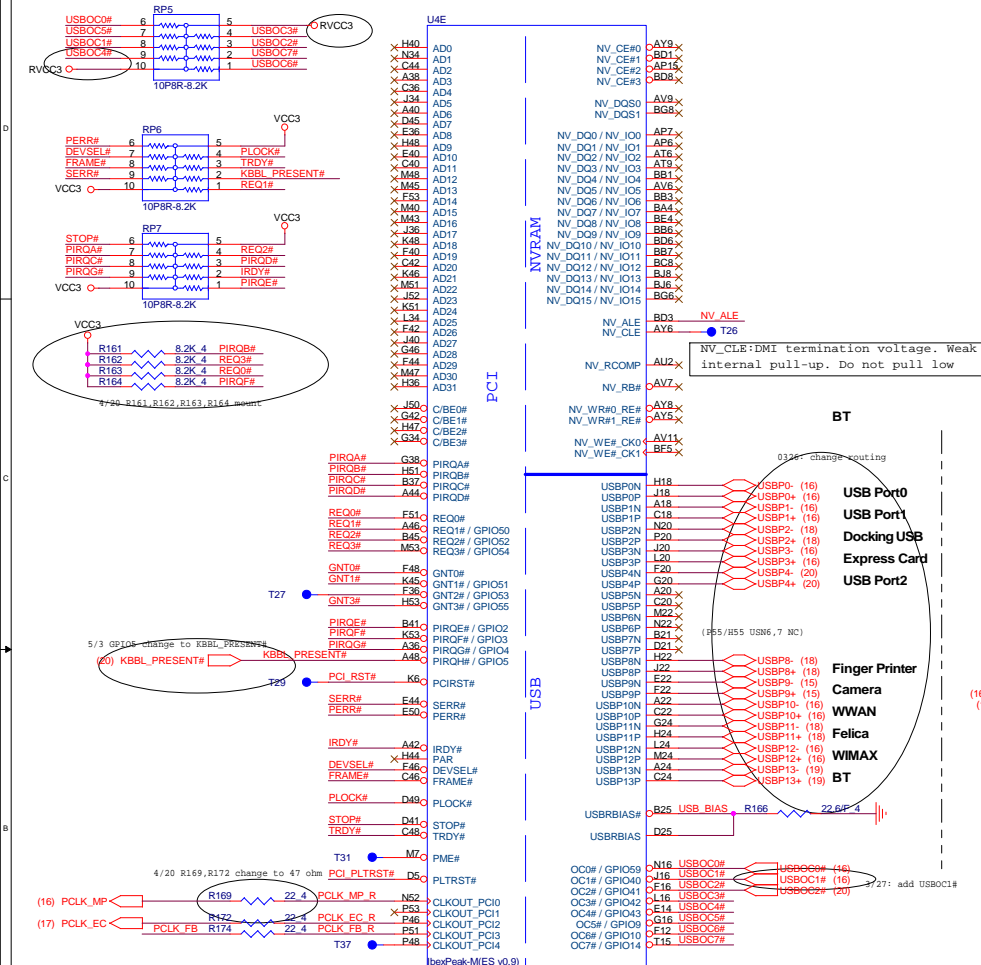
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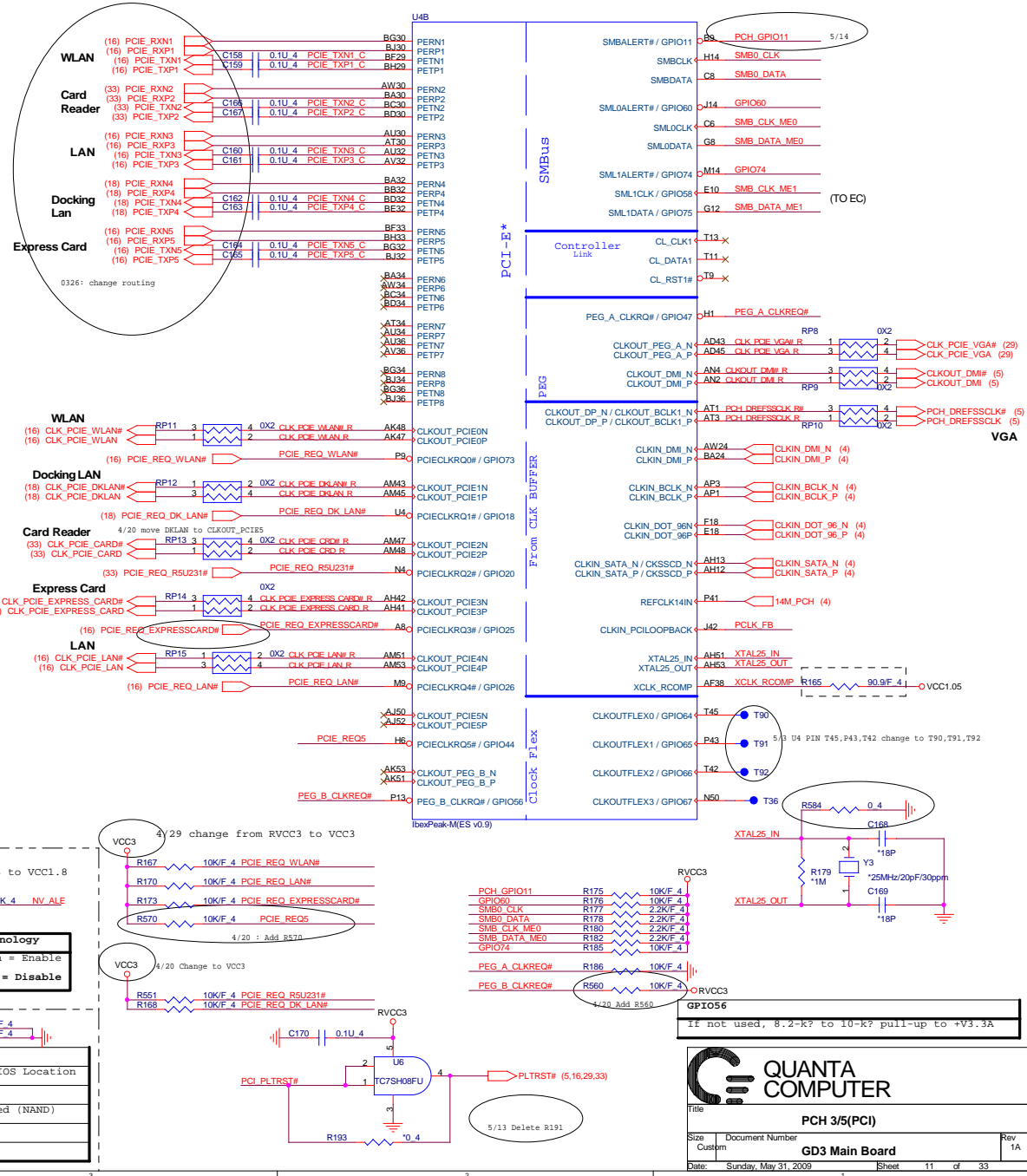




IBEX PEAK-M (PCI,USB,NVRAM)



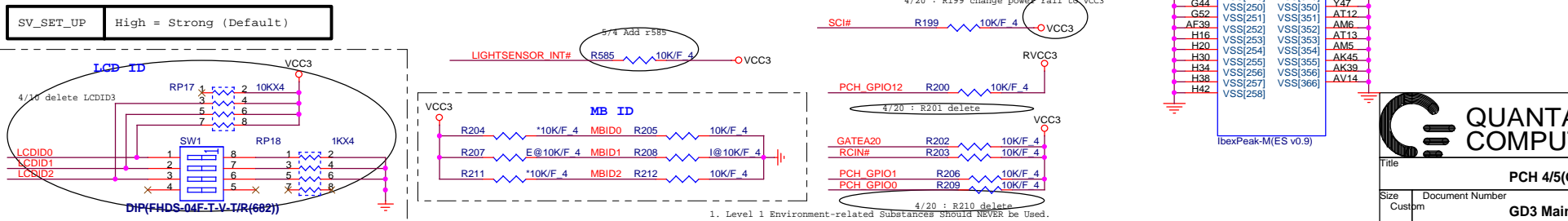
**IBEX PEAK-M (PCI-E, SMBUS, CLK)**





# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)

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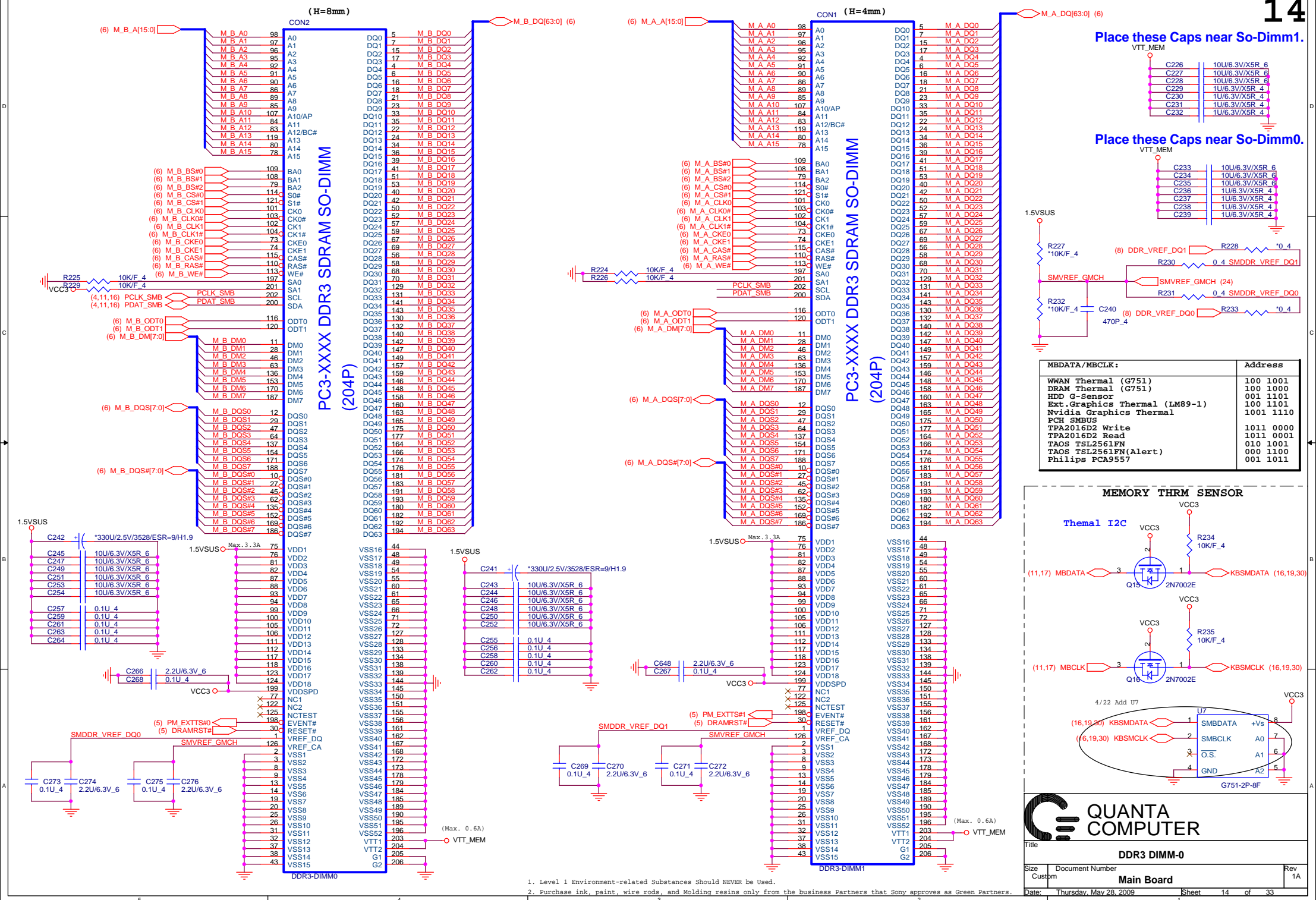
PCH 4/5(GPIO)			Rev 1A
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- Level 1 Environment-related Substances should NEVER be Used.
- Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

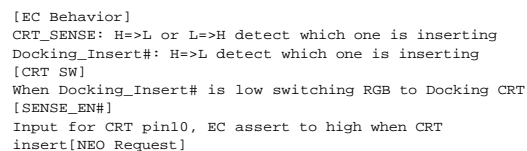
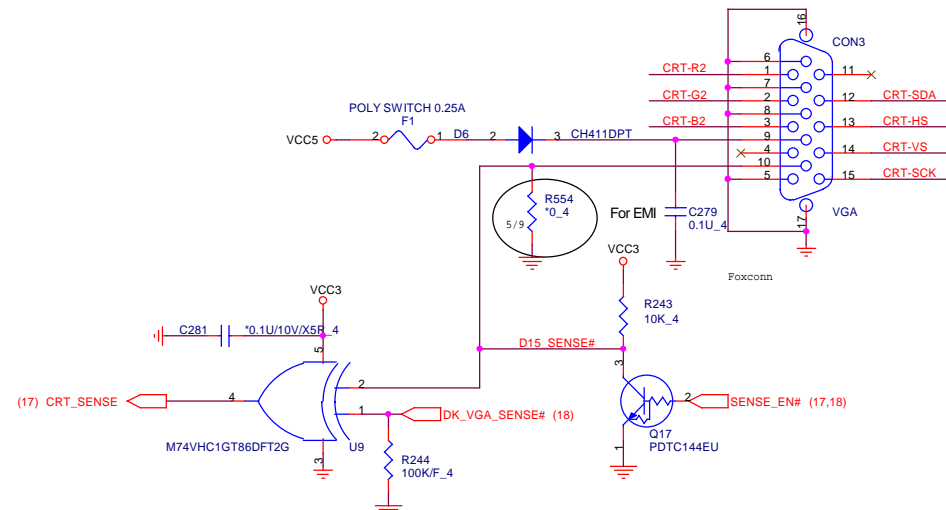


## GD3 Main Board

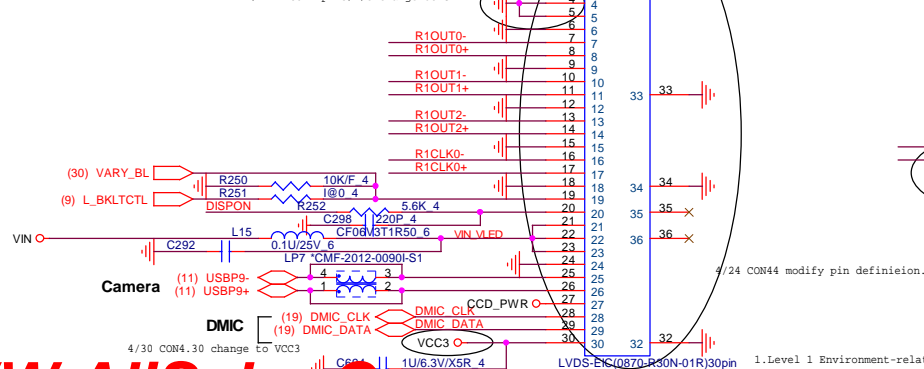
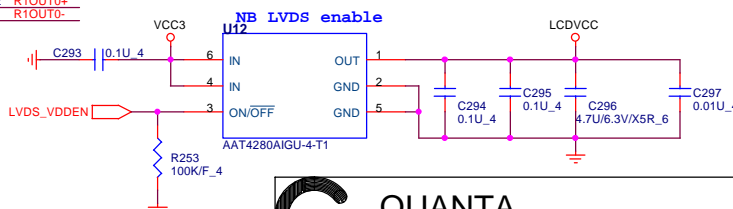
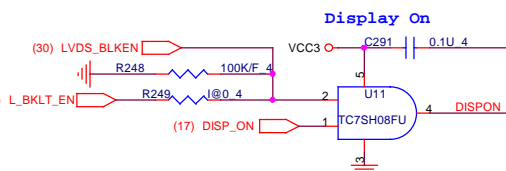
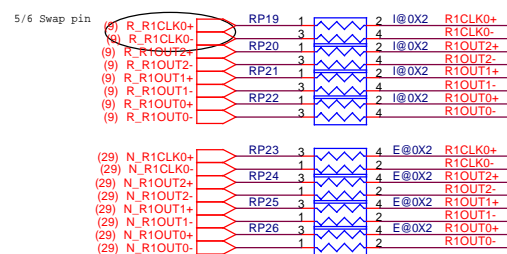
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	SENSE_EN#	DK_VGA_SENSE#	D15_SENSE#	Docking_Insert#	CRT_SENSE#
Without Docking					
MB CRT no Plug	L	L	H	H	L
MB CRT Plug in	L	L	H => L	H	L => H
MB CRT plug out	L	L	L => H	H	H => L
With Docking					
All no Plug	L	L	H	L	L
MB CRT Plug in	L	L	H => L	L	L => H
MB CRT plug out	L	L	L => H	L	H => L
DOCK DVI Plug in	L	H => L	H	L	H => L
DOCK DVI Plug out	L	L => H	H	L	L => H
DOCK CRT Plug	L	H => L	H	L	H => L
DOCK CRT/DVI Plug	L	L => H	H	L	L => H



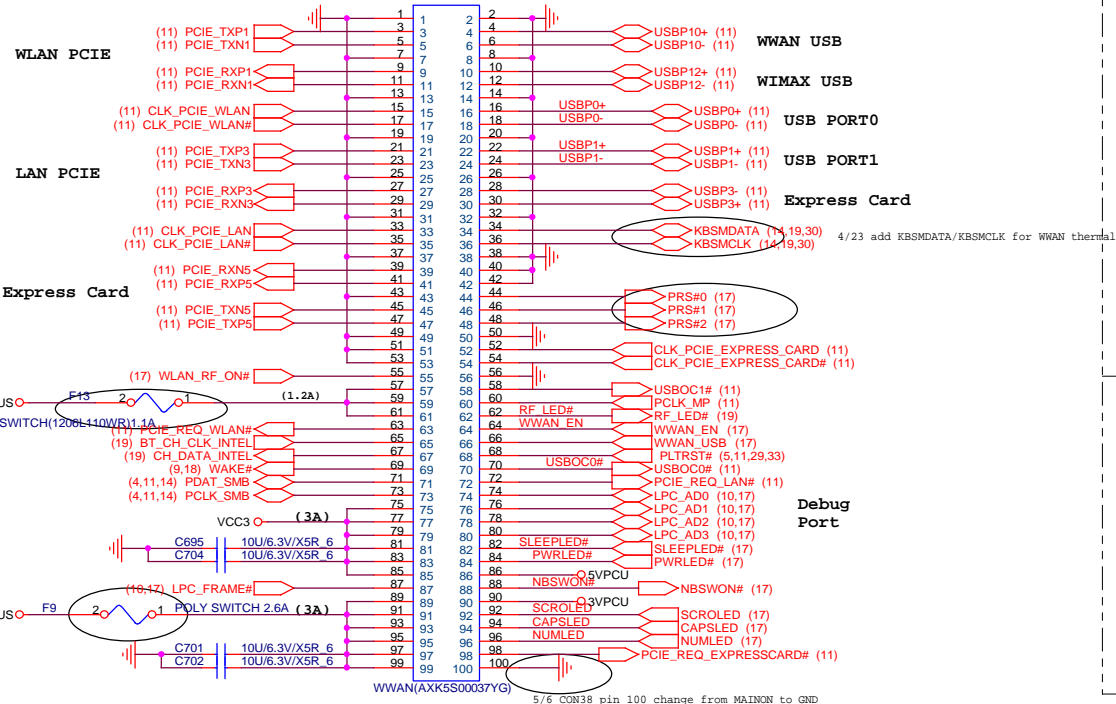
**CRT/LVDS**

## Main Board

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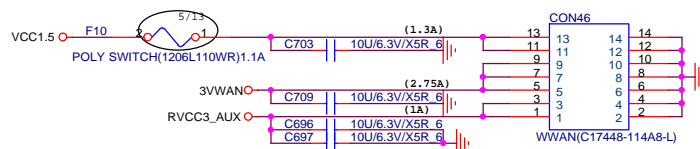
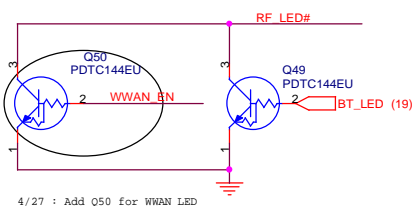
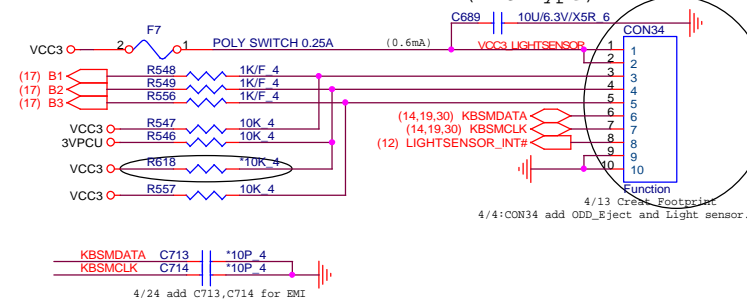
## LAN Board BTB

CON38

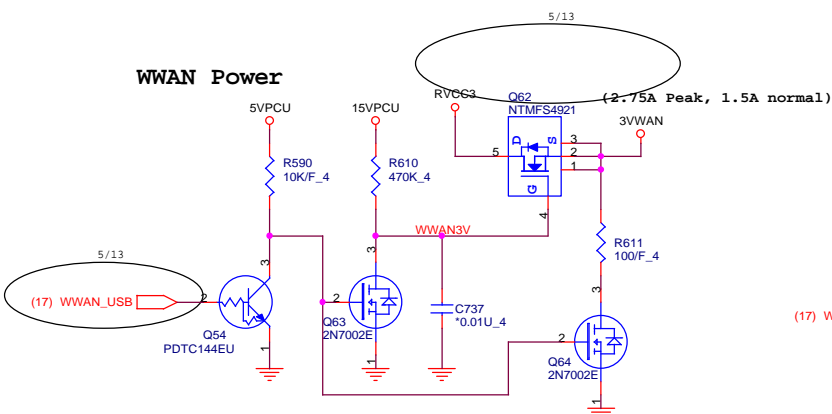


## M/B to Function Board

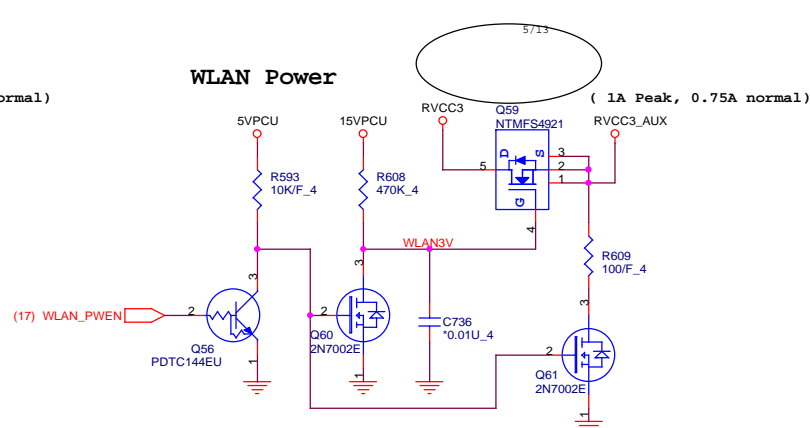
(FFC Type)



## WWAN Power



## WLAN Power

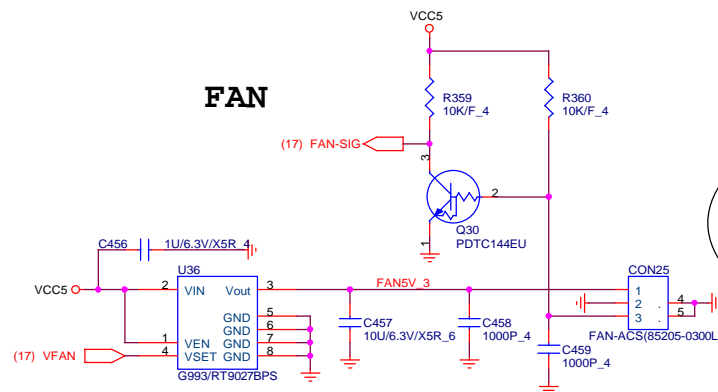
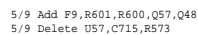
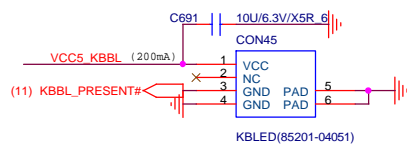
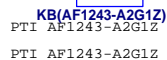








20

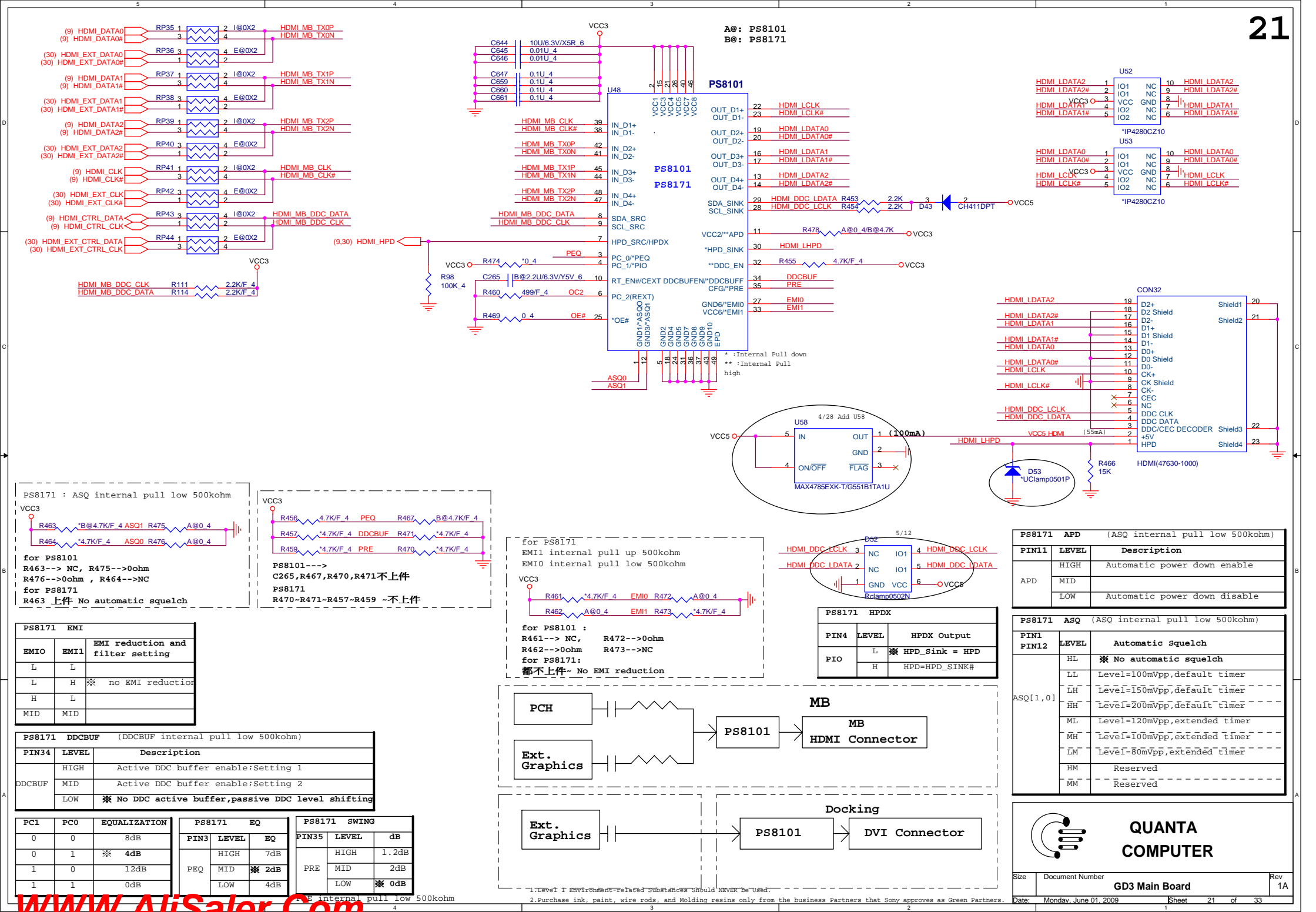


QUANTA  
COMPUTER

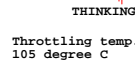
KB/USB/FAN

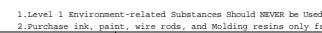
Size	Document Number	Rev
	<b>Main Board</b>	1A
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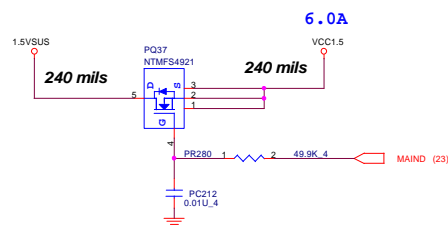
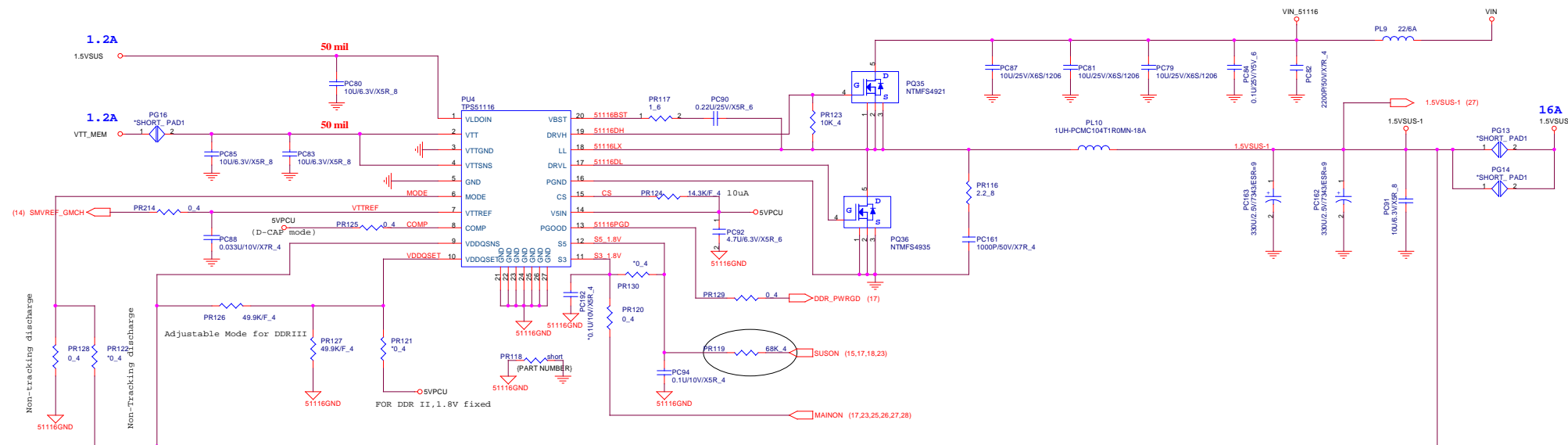








## 1.5VSUS & VTT\_MEM



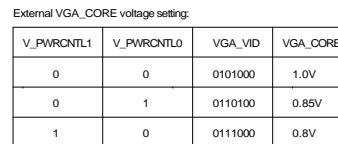
MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

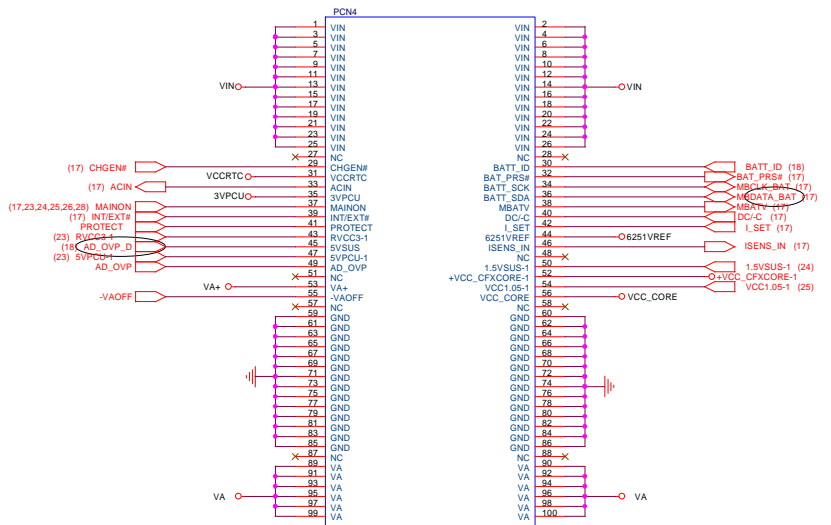
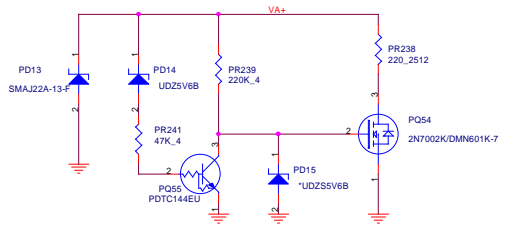
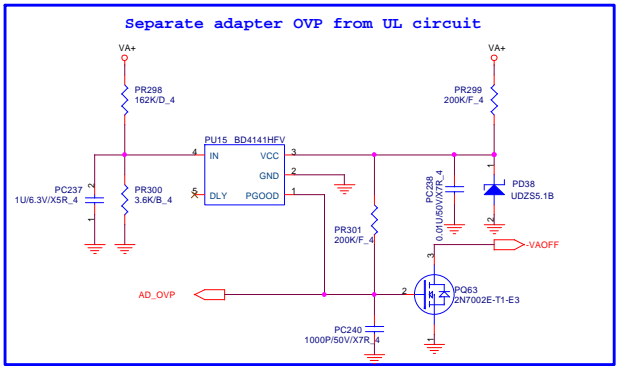
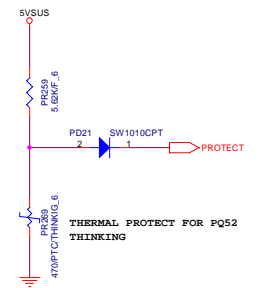
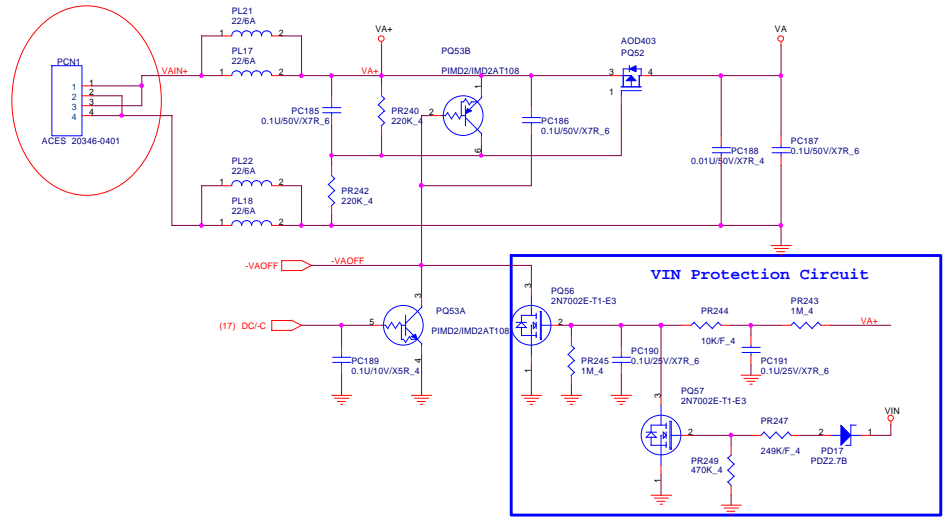
VDDQSET	VDDQ(V)	VTTRF & VTT	NOTE
GND	2.5 fixed	VDDQSNS/2	DDR
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

$$V_{TT} = V_{TTREF} = V_{DDQSNS}/2 = 0.9V$$

STATE	S3	S5	1.8VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off







Charger/B2B-MAT(AKXS00037YG) H=4mm

Quanta P/N

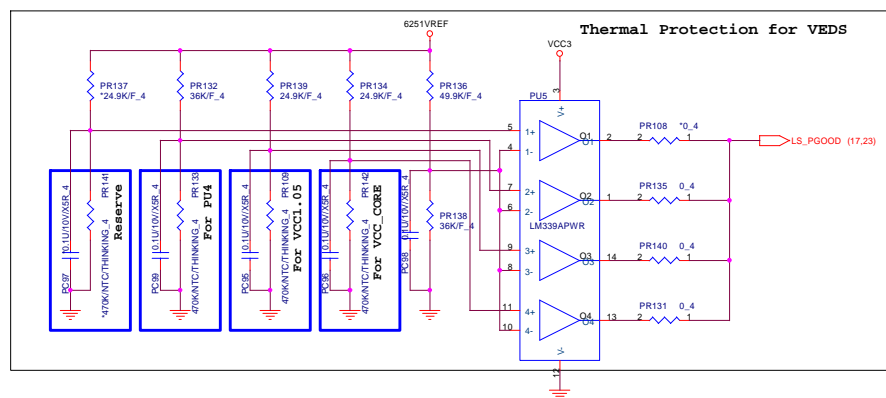
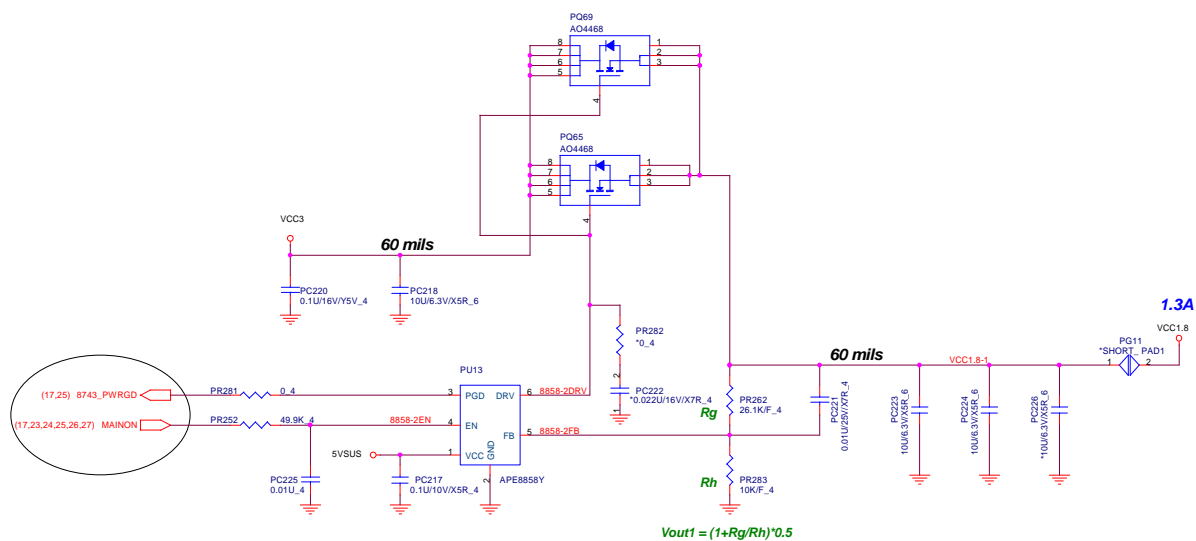
4/18 change pin defined

**QUANTA  
COMPUTER**

Size	Document Number	Rev
	GD3 MB	1A
Date:	Friday, May 15, 2009	Sheet 27 of 33

1. Level 1 Environment-related Substances should NEVER be used.  
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

## VCC1.8



QUANTA  
COMPUTER

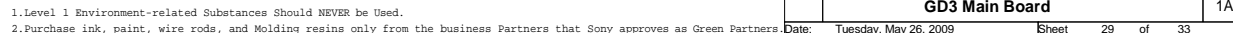
Size	Document Number	Rev
	GD3 Main Board	4A

1. Level 1 Environment-related Substances should NEVER be Used.

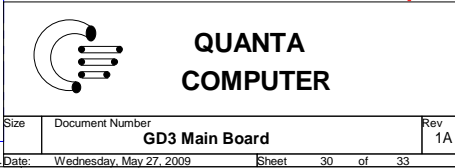
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

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V_PWRCNTL1	V_PWRCNTL0	VGA_VID	VGA_CORE
0	0	0101000	1.0V
0	1	0110100	0.85V
1	0	0111000	0.8V



## Down Side VRAM TOP/BOT

TOP

BOT

U4001C Part 3 of 5

MEMORY INTERFACE

write strobe read strobe

N11M-GE1

4/22 modify to 60.4 ohm according to nVidia PUN

TOP

BOT

Place near U4005

Place near U4006

Place near VRAM side

QUANTA  
COMPUTER

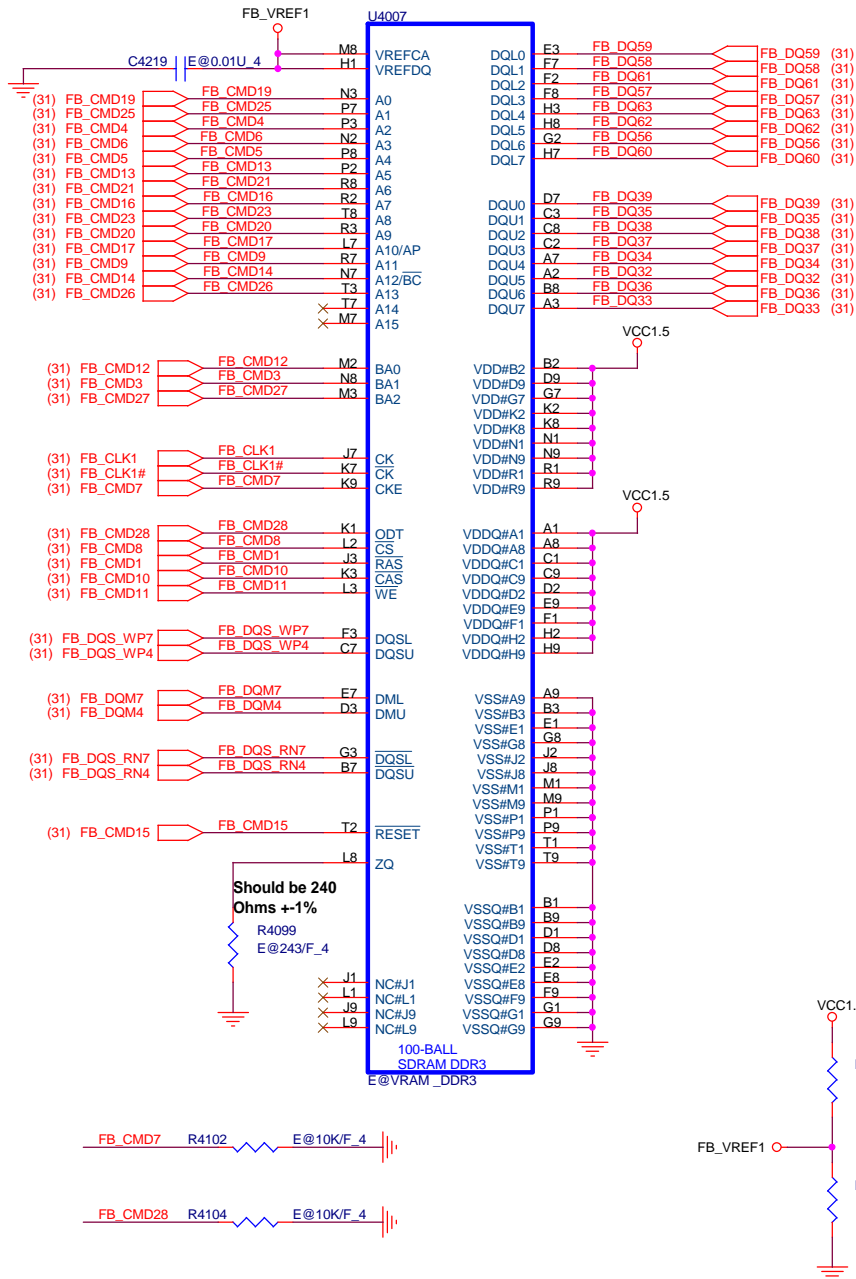
Size	Document Number	Rev
	GD3 Main Board	1A

1. Level 1 Environment-related Substances Should NEVER be Used.

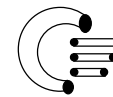
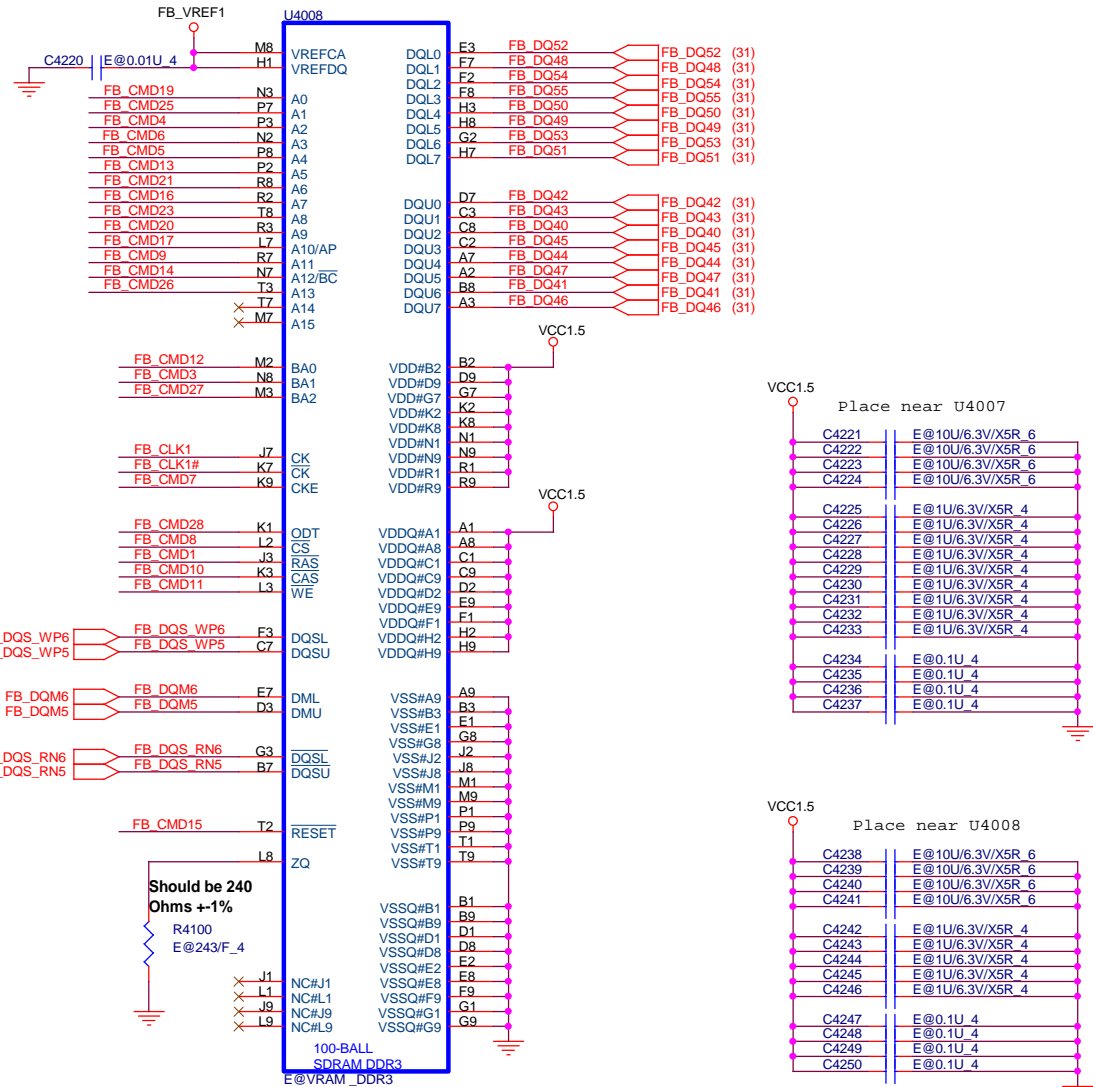
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners. Date: Sunday, May 31, 2009 Sheet 31 of 33

## Up Side VRAM TOP/BOT

TOP



BOT



**QUANTA  
COMPUTER**

1. Level 1 Environment-related Substances Should NEVER be Used.  
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Size	Document Number	Rev
	<b>GD3 Main Board</b>	<b>1A</b>
Date:	Sunday, May 31, 2009	Sheet 32 of 33



